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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/758,863	STASZEWSKI ET AL.	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-47* is/are rejected.

7)☒ Claim(s) *15,18 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1-3, 5-47) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Claim rejection – 35 U.S.C. 102

Applicant asserts that, *"no where, in Wong, is it taught that circuitry within the digital tester 4 manipulates signals from the PLL (DUT 2) to produce a performance metric. Wong teaches that the digital tester 4 can extract and interpret data from the PLL, and includes means for generating a plurality of test patterns and monitoring test results. Col. 1, lines 56-61. However, this is not the same as circuitry contained in the digital tester 4 that manipulates digital signals from the PLL in order to provide a performance metric, as required by claim 32. There is no performance metric that is provided by Wong. In fact, the Examiner does not even point to anything in Wong that would correspond to such a performance metric".*

The examiner respectfully disagrees. The reference of Wong does teach "to enhance accuracy, the digital tester 4 averages several readings of FAP 26. Based on the average reading of FAP 26, the digital tester 4 calculates the expected output frequency (fm) of the PFC 16". (See col. 4, lines 59-65) By averaging several readings of FAP, the tester is somehow manipulating data from the PLL.

Furthermore, the reference of Wong also teaches *"these digital signals are accessible through several on-chip (PLL) read/write ports allowing an external intelligent*

digital circuit (the tester) to compute the PLL dynamic performance" (See col. 1, lines 45-48), *"providing a digital testing approach to measure RXC jitter"* (See col. 4, lines 50-52), and this is done *"by calculating the difference between the measured, PAP 28 readings and the predicted PAP 28 contents"*, and these readings are illustrated in an oscilloscope. (See col. 5, lines 6-16 & fig. 4)

And finally, Wong also teaches a table which lists the various tests necessary to ensure the proper functioning of a typical PLL circuit. (See col. 6, lines 29-36 & Table 2, note that in table 2, a spectrum analyzer is used in order to test FCO clock spectral purity). However, taking the contrary, the examiner has issued a new ground of rejection in order to illustrate that the reference of Wong does, in fact, teaches all of the limitations as claimed.

Claims 1, 3-8, 11, 13-17, 19-22, 24, and 27-31

Applicant further asserts that, *"neither Girardeau nor Yamaguchi teach or suggest manipulating the signal being observed, where the manipulating is done outside of the RF circuit"*.

The examiner respectfully disagrees. The combination of Girardeau and Yamaguchi does teach the limitations as claimed. See office action below for details.

Claims 41, 43, 45, and 46

Applicant further asserts that, *"while Yamaguchi discloses connecting a Spectrum Analyzer to a Phase Detector, it does not disclose or suggest that the*

observed signal is manipulated within the Spectrum Analyzer to generate a performance metric that is, at least in part, based on the manipulation".

The examiner respectfully disagrees. The applicant does disclose, in his specifications, that *"the signal analyzer 1005, which can be integrated onto the same integrated circuits the all-digital frequency synthesizer or transmitter (block 1020), can observe digital signals from within the all-digital frequency synthesizer or transmitter (block 1020) and provide necessary signal processing to generate a performance or compliance metric".* (See paragraph 58) One of ordinary skills in the art would know that a spectrum analyzer is, in fact, a signal analyzer capable of observing, manipulating, and providing performance metrics based on the manipulation.

Claims 1, 3-8, 11, 13-17, 19-22, 24, 27-31, 35, 36, 41, 43, 45, and 46

Applicant further asserts that, *"neither Wong nor Girardeau, whether alone or in combination, teach or suggest each and every limitation of claim 1".*

The examiner respectfully disagrees. These arguments have been already addressed above.

Claims 41, 43, 45, and 46

Applicant further asserts that, *"neither Girardeau nor Wong, whether alone or in combination, teach or suggest observing or manipulating the output of a phase detector in a test circuit outside of the circuit under test. Therefore, the combination of Girardeau and Wong does not teach or suggest each and every limitation of claim 41"*

The examiner respectfully disagrees. These arguments have been already addressed above.

Claim Objections

2. Claims (15, 18, 21) are objected to because of the following informalities:

In Claims 15, 18, 21, the limitation "if" should be rewritten as "when" to avoid the claims from being indefinite. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims (1, 3-8, 11, 13-17, 19-22, 24, 27-31, 41, 43, 45-46) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau)

(US Patent 5,486,792) in view of Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1)

Re claim 1, Girardeau discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit (See fig. 2: 104), wherein the signal has a high degree of correlation with an RF output of the RF circuit (See fig. 1: 24. Furthermore, it is well known in the art that both transmitters and receivers have PLLs)

But the reference of Girardeau fails to specifically disclose that wherein the observing occurs outside of the RF circuit; manipulating the signal outside of the RF circuit; and producing a metric for the test outside of the RF circuit based on results from the manipulating.

However, Yamaguchi does. (See fig. 29) Yamaguchi discloses a spectrum analyzer connected to the output of the phase detector, and located outside an RF circuit and a PLL. One skilled in the art would know that the spectrum analyzer (signal analyzer) is capable of observing, manipulating, and generating performance metrics.

Therefore, taking the combined teachings of Girardeau and Yamaguchi as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, in the manner as claimed and as taught by Yamaguchi, for the benefit of optimizing the performance of the PLL.

Re claim 3, the combination of Girardeau and Yamaguchi further discloses that wherein the signal is a phase error signal. (In Girardeau, see fig. 1: 12, col. 2, lines 50-56)

Re claim 4, the combination of Girardeau and Yamaguchi further discloses that wherein the signal has a high degree of correlation with an RF output of the RF circuit. (In Girardeau, see fig. 1: 24. Furthermore, one skilled in the art would know that the frequency of the error signal is within the cut-off frequency of the loop filter, thus achieving a high degree of correlation.)

Re claim 6, the combination of Girardeau and Yamaguchi further discloses that wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. (In Girardeau, see fig. 1 & col. 2, lines 54-56)

Re claim 7, the combination of Girardeau and Yamaguchi further discloses that wherein the signal is an output of a phase detector. (In Girardeau, see fig. 1 & col. 2, lines 54-56)

Re claim 8, the combination of Girardeau and Yamaguchi further discloses that wherein the signal has been filtered. (In Girardeau, see fig. 1: 24 & col. 2, lines 62-65)

Re claim 11, the combination of Girardeau and Yamaguchi further discloses that wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter. (In Girardeau, see fig. 1: 24 & col. 2, lines 62-65)

Re claim 13, the combination of Girardeau and Yamaguchi further discloses that wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. (One skilled in the art would know that the frequency of the error signal, outputted from the phase comparator, is less than the RF frequency.)

Re claim 14, the combination of Girardeau and Yamaguchi further discloses that wherein the test is for phase error trajectory and the signal is the output of a phase detector (In Girardeau, see fig. 1 & col. 2, lines 54-56), and wherein the manipulation comprises measuring a change in the signal. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 15, the combination of Girardeau and Yamaguchi further discloses that wherein if the change in the signal is less than a specified threshold, then the phase error trajectory is good. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 16, the combination of Girardeau and Yamaguchi further discloses that wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 17, the combination of Girardeau and Yamaguchi further discloses that wherein the test is for frequency lock and the signal is the output of a phase detector (In Girardeau, see col. 2, lines 30-37 & col. 4, lines 65-67), and wherein the manipulation comprises comparing a value of the signal over several samples. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold. Furthermore, during tracking mode the PLL tries to keep the phase locked.)

Re claim 19, the combination of Girardeau and Yamaguchi further discloses that wherein the samples are taken at different times. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold. Furthermore, during tracking mode the PLL tries to keep the phase locked.)

Re claim 20, the combination of Girardeau and Yamaguchi further discloses that wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter (In Girardeau, see col. 5, lines 19-21), and wherein the manipulation comprises comparing the signal with a specified range. (In Girardeau, see

col. 2, lines 30-36. The error signal is being compared with the threshold.)

Re claim 21, the combination of Girardeau and Yamaguchi further discloses that wherein if the signal is within the specified range, then the frequency deviation is within acceptable limits. (In Girardeau, see col. 2, lines 30-36)

Re claim 22, the combination of Girardeau and Yamaguchi further discloses that wherein the manipulation further comprises comparing several samples of the signal. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Re claim 27, the combination of Girardeau and Yamaguchi further discloses that wherein the RF circuit is an all-digital frequency synthesizer. (In Girardeau, see col. 5, line 20)

Re claim 28, the combination of Girardeau and Yamaguchi further discloses that wherein the RF circuit is an all-digital transmitter. (In Girardeau, see col. 1, lines 24-27)

Re claim 29, the combination of Girardeau and Yamaguchi further discloses that wherein the transmitter is used in a wireless communications network. (In Girardeau, see col. 1, lines 24-27)

Re claim 30, the combination of Girardeau and Yamaguchi further discloses that wherein the wireless communications network is Bluetooth compliant. (In Girardeau, see col. 1, lines 24-27. One of ordinary skills in the art would know that the network is Bluetooth compliant.)

Re claim 31, the combination of Girardeau and Yamaguchi further discloses that wherein the testing comprises a functional test or a compliance test of the RF circuit. (In Girardeau, see col. 2, lines 30-37 & col. 5, lines 10-21)

Claim 41 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 41. Therefore, claim 41 has been analyzed and rejected w/r to claim 1 above.

Re claim 43, the combination of Girardeau and Yamaguchi further discloses a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase. (In Girardeau, see fig. 1: 24)

2. **Claims (5) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) in view of Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1)**

Re claim 5, the combination of Girardeau and Yamaguchi fails to explicitly teach that that wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest.

However, the reference of Girardeau does suggest the teaching of a lock indicator for indicating when the PLL is in a lock mode. Furthermore, one skilled in the art would know that, when the PLL is in a lock mode the output signal and the input signal are the same, thus, exhibiting a transfer function which is flat.)

Therefore, it would have obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, as modified by Yamaguchi, for the benefit of indicating when the PLL is in lock mode.

3. **Claims (24) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 1 above, and further in view of Skierszkan et al. (hereinafter Skierszkan) (US Publication 2002/0001359 A1)**

Re claim 24, the combination of Girardeau and Yamaguchi further discloses that wherein the RF circuit contains an all-digital phase-locked loop. (In Girardeau, see fig. 1)

But the combination of Girardeau and Yamaguchi fails to explicitly teach that the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth.

However, Skierszkan does. (See paragraph 57) Skierszkan discloses an acquisition PLL that has a low pass filter with a relatively high cut-off frequency. The acquisition PLL tracks all changes in the input signal, including error components.

Therefore, taking the combined teachings of Girardeau, Yamaguchi, and Skierszkan as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, as modified by Yamaguchi, in the manner as claimed and as taught by Skierszkan, for the benefit of achieving acquisition. (See paragraph 57)

Claims (45) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claims 1 & 41 above, and further in view of Ko. (US Patent 5,982,832)

Re claim 45, the combination of Girardeau and Yamaguchi fails to disclose that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion.

However, Ko does. (See fig. 4 & col. 4, lines 18-25) Ko discloses a plurality of filters arranged in a parallel fashion.

Therefore, taking the combined teachings of Girardeau, Yamaguchi, and Ko as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, as modified by Yamaguchi, in the

manner as claimed and as taught by Ko, for the benefit of achieving phase compensation.

Claims (46) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claims 1 & 41 above, and further in view of Cucchietti et al. (hereinafter Cucchietti) (US Patent 4,819,080)

Re claim 46, the combination of Girardeau and Yamaguchi fails to disclose that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion.

However, Cucchietti does. (See fig. 4: "BP" & col. 2, lines 45-52) Cucchietti discloses two cascaded filters located at the output of a phase detector.

Therefore, taking the combined teachings of Girardeau, Yamaguchi, and Cucchietti as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, as modified by Yamaguchi, in the manner as claimed and as taught by Cucchietti, for the benefit of achieving passing the desired frequencies and eliminating the non-desired frequencies.

1. **Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al.**

(hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 1 above, and further in view of Kim et al (hereinafter Kim) (US Patent 6,885,700 B1).

Re claim 2, the combination of Girardeau and Yamaguchi fails to specifically disclose that wherein the testing is performed using built-in self-test (BIST) techniques.

However, Kim does. (See abstract & col. 1, lines 13-40) Kim discloses a charge-based frequency technique that performs structural and defect-oriented testing and uses existing blocks to save die area.

Therefore, taking the combined teachings of Girardeau, Yamaguchi & Kim as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system of Girardeau, as modified by Yamaguchi, in the manner as claimed and as taught by Kim, for the benefit of providing proper stimulus for the loop filter located inside the PLL.

Claims (10 & 44) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 1 above, and further in view of Mathe et al (hereinafter Mathe) (US Patent 5,825,253).

Re claim 10, the combination of Girardeau and Yamaguchi fails to specifically disclose that wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter.

However, Mathe does. (See col. 5, lines 32-37) Mathe discloses a phase lock loop that contains a loop filter which can be implemented as a digital filter such as an infinite impulse response (IIR) filter.

Therefore, taking the combined teachings of Girardeau, Yamaguchi & Mathe as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Yamaguchi, in the manner as claimed, and as taught by Mathe, for the benefit of providing synthesis of both zeros and poles in the filter. (See col. 9, lines 55-56)

Re claim 44, the motivation for combining these two references has already been established in claim 10 above, therefore, the combination of Girardeau, Yamaguchi and Mathe further discloses that wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof. (In Mathe, see col. 5, lines 32-37 & col. 9, lines 55-56)

Claims (12 & 47) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claims 1 & 41 above, and further in view of Koshiro et al (hereinafter Koshiro) (US Patent 5,768,326).

Re claim 12, the combination of Girardeau and Yamaguchi fails to specifically disclose that wherein the signal is an output of a gain normalization block.

However, Koshiro does. (See fig. 3: 31 & col. 11, lines 3-9) Koshiro discloses a PLL circuit where it is possible to normalized the output of the substractor, which is a diffrerence between PCR and the output of the counter. This normalization passes through the low-pass filter and is able to control the VCXO accurately.

Therefore, taking the combined teachings of Girardeau, Yamaguchi, and Koshiro as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Yamaguchi, in the manner as claimed, and as taught by Koshiro, for the benefit of controlling the VCXO accurately. (See col. 11, lines 3-9).

Re claim 47, the motivation for combining these two references has already been established in claim 10 above, therefore, the combination of Girardeau, Yamaguchi and Koshiro further disclose a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO. (The references of Girardeau and Mathe disclose this limitation. Girardeau teaches a DPLL having a phase detector followed by a DCO. On the other hand, Koshiro teaches a normalization unit coupled in between a phase detector and a VCO. As a whole, these two references meet the limitations as claimed.)

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al.

(hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 1 above, and further in view of Gustafson et al (hereinafter Gustafson) (US Patent 4,086,539).

Re claim 18, the combination of Girardeau and Yamaguchi fails to specifically disclose that wherein if a variance in the magnitude is less than a specified threshold, then the frequency has been locked.

However, Gustafson does. (See abstract & col. 1, lines 37-40) Gustafson discloses that phase lock loops produce favorable results in terms of phase-error variance in high frequency system and below threshold.

Therefore, taking the combined teachings of Girardeau, Yamaguchi & Gustafson as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Yamaguchi, in the manner as claimed, and as taught by Gustafson, for the benefit of locking the frequency.

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claim 41 above, and further in view of Knudsen (US Patent 7,079,611 B2).

Re claim 42, the combination of Girardeau and Yamaguchi fails to specifically disclose a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock.

However, Knudsen does. (See fig. 1 & col. 2, lines 14-25) Knudsen discloses a digital phase lock loop that computes the time difference of the clock input and the clock output.

Therefore, taking the combined teachings of Girardeau, Yamaguchi & Knudsen as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau in the manner as claimed, and as taught by Knudsen, for the benefit of providing useful information to a filter, which will be later on, to achieve synchronization. (See col. 2, lines 20-25)

4. Claims (32, 34, 36-40) are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (hereinafter Wong) (US Patent 5,295,079)

Re claim 32, Wong discloses a circuit comprising: a processor coupled to a radio frequency (RF) circuit. (See fig. 2)

But the reference of Wong fails to explicitly teach that the processor containing circuitry to manipulate digital signals from the RF circuit to provide a performance metric for the RF circuit; and a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals.

However, the reference of Wong does suggest that the teachings of digital tester (an intelligent digital controller) coupled to an input "keyboard" (See fig. 1: the input of element 4 & col. 1, lines 56-61), that performs tests, extract, and interpret data from the device under test (DUT). Furthermore, table 2 shows several of how to test some PLL

dynamic performance parameters. (See fig. 2: 4 & col. 1, lines 45-48, 56-61, col. 2, lines 36-40, col. 4, lines 6-15)

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of testing some PLL dynamic performance parameters. (See col. 6, lines 29-31)

Re claim 34, the combination of Wong further discloses that wherein the RF circuit is integrated onto a first integrated circuit, wherein the processor is integrated onto a second integrated circuit. (In Wong, see fig. 2)

Re claim 36, the combination of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector. (In Wong, see fig. 2)

Re claim 37, the combination of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to a filtered output of a phase detector. (In Wong, see fig. 2: 24 & col. 3, lines 19-22, 50-56)

Re claim 38, the combination of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector and a filtered output of a phase detector. (In Wong, see

fig. 2 & col. 3, lines 50-55)

Re claim 39, the combination of Wong further discloses that wherein the circuit permits the testing of the RF circuit in wafer, in packaged integrated circuit, in factory, and in field. (In Wong, see col. 1, lines 38-41, 48-51 & col. 4, lines 16-27)

Re claim 40, the combination of Wong further discloses that wherein the circuit permits the testing of the RF circuit, and wherein the testing is of a type selected from a group consisting of a phase trajectory error, a frequency lock, a frequency deviation, a phase noise power, or combinations thereof. (In Wong, see fig. 2, 4b & 4c & col. 4, line 34 – col. 6, line 35 & table 2)

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (hereinafter Wong) (US Patent 5,295,079)

Re claim 33, the reference of Wong fails to disclose a latch coupled to the processor, the latch to store the performance metric provided by the processor.

However, the reference of Wong does suggest the teaching of a digital tester, which may be a hand-held microprocessor-based controller with a keyboard and a multi-digit display that can be used for network servicing or for low-cost lab-quality engineering setups. (See col. 4, lines 13-16) Furthermore, one skilled in the art would know that latches may be used as storage elements, from which flip-flops are usually

constructed. And registers, which are used extensively in the design of digital systems for storing data, consists of a set of flip-flops.

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of testing some PLL dynamic performance parameters. (See col. 6, lines 29-31)

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (hereinafter Wong) (US Patent 5,295,079)

Re claim 35, the reference of Wong fails to explicitly teach that wherein the first and the second integrated circuit are the same integrated circuit.

However, the reference of Wong does suggest the teaching of a IO controller integrated within the same integrated circuit as the RF circuit. (See fig. 2: 22 & 25)

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of minimizing the time delay.

5. Claims (1, 3-8, 11, 13-17, 19-22, 24, 27-31, 41, 43, 45-46) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) in view of Wong et al. (hereinafter Wong) (US Patent 5,295,079)

6. Re claim 1, Girardeau discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit, wherein the signal is a digital

signal from within a processing portion of the RF circuit (See fig. 2: 104), wherein the signal has a high degree of correlation with an RF output of the RF circuit (See fig. 1: 24. Furthermore, it is well known in the art that both transmitters and receivers have PLLs)

But the reference of Girardeau fails to specifically disclose that wherein the observing occurs outside of the RF circuit; manipulating the signal outside of the RF circuit; and producing a metric for the test outside of the RF circuit based on results from the manipulating.

However, Wong does. The reference of Wong does teach "to enhance accuracy, the digital tester 4 averages several readings of FAP 26. Based on the average reading of FAP 26, the digital tester 4 calculates the expected output frequency (fm) of the PFC 16". (See col. 4, lines 59-65) By averaging several readings of FAP, the tester is somehow manipulating data from the PLL.

Furthermore, the reference of Wong also teaches "these digital signals are accessible through several on-chip (PLL) read/write ports allowing an external intelligent digital circuit (the tester) to compute the PLL dynamic performance" (See col. 1, lines 45-48), "providing a digital testing approach to measure RXC jitter" (See col. 4, lines 50-52), and this is done "by calculating the difference between the measured, PAP 28 readings and the predicted PAP 28 contents", and these readings are illustrated in an oscilloscope. (See col. 5, lines 6-16 & fig. 4)

And finally, Wong also teaches a table which lists the various tests necessary to ensure the proper functioning of a typical PLL circuit. (See col. 6, lines 29-36 & Table 2)

Please note that in table 2, a spectrum analyzer is used in order to test FCO clock spectral purity). One skilled in the art would know that the spectrum analyzer (signal analyzer) is capable of observing, manipulating, and generating performance metrics.

Therefore, taking the combined teachings of Girardeau and Wong as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, in the manner as claimed and as taught by Wong, for the benefit of optimizing the performance of the PLL.

Re claim 3, the combination of Girardeau and Wong further discloses that wherein the signal is a phase error signal. (In Girardeau, see fig. 1: 12, col. 2, lines 50-56)

Re claim 4, the combination of Girardeau and Wong further discloses that wherein the signal has a high degree of correlation with an RF output of the RF circuit. (In Girardeau, see fig. 1: 24. Furthermore, one skilled in the art would know that the frequency of the error signal is within the cut-off frequency of the loop filter, thus achieving a high degree of correlation.)

Re claim 6, the combination of Girardeau and Wong further discloses that wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. (In Girardeau, see fig. 1

& col. 2, lines 54-56)

Re claim 7, the combination of Girardeau and Wong further discloses that wherein the signal is an output of a phase detector. (In Girardeau, see fig. 1 & col. 2, lines 54-56)

Re claim 8, the combination of Girardeau and Wong further discloses that wherein the signal has been filtered. (In Girardeau, see fig. 1: 24 & col. 2, lines 62-65)

Re claim 11, the combination of Girardeau and Wong further discloses that wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter. (In Girardeau, see fig. 1: 24 & col. 2, lines 62-65)

Re claim 13, the combination of Girardeau and Wong further discloses that wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. (One skilled in the art would know that the frequency of the error signal, outputted from the phase comparator, is less than the RF frequency.)

Re claim 14, the combination of Girardeau and Wong further discloses that wherein the test is for phase error trajectory and the signal is the output of a phase detector (In Girardeau, see fig. 1 & col. 2, lines 54-56), and wherein the manipulation

comprises measuring a change in the signal. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 15, the combination of Girardeau and Wong further discloses that wherein if the change in the signal is less than a specified threshold, then the phase error trajectory is good. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 16, the combination of Girardeau and Wong further discloses that wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. (In Girardeau, see fig. 2: error signal. And see col. 5, lines 37-39)

Re claim 17, the combination of Girardeau and Wong further discloses that wherein the test is for frequency lock and the signal is the output of a phase detector (In Girardeau, see col. 2, lines 30-37 & col. 4, lines 65-67), and wherein the manipulation comprises comparing a value of the signal over several samples. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold. Furthermore, during tracking mode the PLL tries to keep the phase locked.)

Re claim 19, the combination of Girardeau and Wong further discloses that wherein the samples are taken at different times. (In Girardeau, see fig. 2 & col. 5, lines

37-40. The error signal is being compared with the threshold. Furthermore, during tracking mode the PLL tries to keep the phase locked.)

Re claim 20, the combination of Girardeau and Wong further discloses that wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter (In Girardeau, see col. 5, lines 19-21), and wherein the manipulation comprises comparing the signal with a specified range. (In Girardeau, see col. 2, lines 30-36. The error signal is being compared with the threshold.)

Re claim 21, the combination of Girardeau and Wong further discloses that wherein if the signal is within the specified range, then the frequency deviation is within acceptable limits. (In Girardeau, see col. 2, lines 30-36)

Re claim 22, the combination of Girardeau and Wong further discloses that wherein the manipulation further comprises comparing several samples of the signal. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Re claim 27, the combination of Girardeau and Wong further discloses that wherein the RF circuit is an all-digital frequency synthesizer. (In Girardeau, see col. 5, line 20)

Re claim 28, the combination of Girardeau and Wong further discloses that wherein the RF circuit is an all-digital transmitter. (In Girardeau, see col. 1, lines 24-27)

Re claim 29, the combination of Girardeau and Wong further discloses that wherein the transmitter is used in a wireless communications network. (In Girardeau, see col. 1, lines 24-27)

Re claim 30, the combination of Girardeau and Wong further discloses that wherein the wireless communications network is Bluetooth compliant. (In Girardeau, see col. 1, lines 24-27. One of ordinary skills in the art would know that the network is Bluetooth compliant.)

Re claim 31, the combination of Girardeau and Wong further discloses that wherein the testing comprises a functional test or a compliance test of the RF circuit. (In Girardeau, see col. 2, lines 30-37 & col. 5, lines 10-21)

Claim 41 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 41. Therefore, claim 41 has been analyzed and rejected w/r to claim 1 above.

Re claim 43, the combination of Girardeau and Yamaguchi further discloses a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired

amount of attenuation to the computed difference between the reference phase and the variable phase. (In Girardeau, see fig. 1: 24)

7. Claims (5) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) in view of Wong et al. (hereinafter Wong) (US Patent 5,295,079)

8. Re claim 5, the combination of Girardeau and Wong fails to explicitly teach that that wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest.

However, the reference of Girardeau does suggest the teaching of a lock indicator for indicating when the PLL is in a lock mode. Furthermore, one skilled in the art would know that, when the PLL is in a lock mode the output signal and the input signal are the same, thus, exhibiting a transfer function which is flat.)

Therefore, it would have obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, as modified by Wong, for the benefit of indicating when the PLL is in lock mode.

9. **Claims (24) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Skierszkan et al. (hereinafter Skierszkan) (US Publication 2002/0001359 A1)**

Re claim 24, the combination of Girardeau and Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop. (In Girardeau, see fig. 1)

But the combination of Girardeau and Wong fails to explicitly teach that the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth.

However, Skierszkan does. (See paragraph 57) Skierszkan discloses an acquisition PLL that has a low pass filter with a relatively high cut-off frequency. The acquisition PLL tracks all changes in the input signal, including error components.

Therefore, taking the combined teachings of Girardeau, Wong, and Skierszkan as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, as modified by Wong, in the manner as claimed and as taught by Skierszkan, for the benefit of achieving acquisition. (See paragraph 57)

10. **Claims (45) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claims 1 & 41 above, and further in view of Ko. (US Patent 5,982,832)**

Re claim 45, the combination of Girardeau and Wong fails to disclose that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion.

However, Ko does. (See fig. 4 & col. 4, lines 18-25) Ko discloses a plurality of filters arranged in a parallel fashion.

Therefore, taking the combined teachings of Girardeau, Wong, and Ko as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, as modified by Wong, in the manner as claimed and as taught by Ko, for the benefit of achieving phase compensation.

11. **Claims (46) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claims 1 & 41 above, and further in view of Cucchietti et al. (hereinafter Cucchietti) (US Patent 4,819,080)**

Re claim 46, the combination of Girardeau and Wong fails to disclose that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion.

However, Cucchietti does. (See fig. 4: "BP" & col. 2, lines 45-52) Cucchietti discloses two cascaded filters located at the output of a phase detector.

Therefore, taking the combined teachings of Girardeau, Wong, and Cucchietti as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Girardeau, as modified by Wong, in the manner as claimed and as taught by Cucchietti, for the benefit of achieving passing the desired frequencies and eliminating the non-desired frequencies.

2. **Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Kim et al (hereinafter Kim) (US Patent 6,885,700 B1).**

Re claim 2, the combination of Girardeau and Wong fails to specifically disclose that wherein the testing is performed using built-in self-test (BIST) techniques.

However, Kim does. (See abstract & col. 1, lines 13-40) Kim discloses a charge-based frequency technique that performs structural and defect-oriented testing and uses existing blocks to save die area.

Therefore, taking the combined teachings of Girardeau, Wong & Kim as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system of Girardeau, as modified by Wong, in the manner as claimed and as taught by Kim, for the benefit of providing proper stimulus for the loop filter located inside the PLL.

12. **Claims (10 & 44) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Mathe et al (hereinafter Mathe) (US Patent 5,825,253).**

Re claim 10, the combination of Girardeau and Wong fails to specifically disclose that wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter.

However, Mathe does. (See col. 5, lines 32-37) Mathe discloses a phase lock loop that contains a loop filter which can be implemented as a digital filter such as an infinite impulse response (IIR) filter.

Therefore, taking the combined teachings of Girardeau, Wong & Mathe as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Wong, in the manner as claimed, and as taught by Mathe, for the benefit of providing synthesis of both zeros and poles in the filter. (See col. 9, lines 55-56)

Re claim 44, the motivation for combining these two references has already been established in claim 10 above, therefore, the combination of Girardeau, Wong and Mathe further discloses that wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof. (In Mathe, see col. 5, lines 32-37 & col. 9, lines 55-56)

13. **Claims (12 & 47) are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claims 1 & 41 above, and further in view of Koshiro et al (hereinafter Koshiro) (US Patent 5,768,326).**

Re claim 12, the combination of Girardeau and Wong fails to specifically disclose that wherein the signal is an output of a gain normalization block.

However, Koshiro does. (See fig. 3: 31 & col. 11, lines 3-9) Koshiro discloses a PLL circuit where it is possible to normalized the output of the substractor, which is a diffrerence between PCR and the output of the counter. This normalization passes through the low-pass filter and is able to control the VCXO accurately.

Therefore, taking the combined teachings of Girardeau, Wong, and Koshiro as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Wong, in the manner as claimed, and as taught by Koshiro, for the benefit of controlling the VCXO accurately. (See col. 11, lines 3-9).

Re claim 47, the motivation for combining these two references has already been established in claim 10 above, therefore, the combination of Girardeau, Wong and Koshiro further disclose a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO. (The references of Girardeau and Mathe disclose this limitation. Girardeau teaches a DPLL having a phase detector followed by a DCO. On the other hand, Koshiro teaches a normalization unit coupled in between a phase detector and a VCO. As a whole, these two references meet the limitations as claimed.)

14. **Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al.**

(hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Gustafson et al (hereinafter Gustafson) (US Patent 4,086,539).

Re claim 18, the combination of Girardeau and Wong fails to specifically disclose that wherein if a variance in the magnitude is less than a specified threshold, then the frequency has been locked.

However, Gustafson does. (See abstract & col. 1, lines 37-40) Gustafson discloses that phase lock loops produce favorable results in terms of phase-error variance in high frequency system and below threshold.

Therefore, taking the combined teachings of Girardeau, Wong & Gustafson as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Wong, in the manner as claimed, and as taught by Gustafson, for the benefit of locking the frequency.

15. **Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US patent 5,486,792) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 41 above, and further in view of Knudsen (US Patent 7,079,611 B2).**

Re claim 42, the combination of Girardeau and Wong fails to specifically disclose a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock.

However, Knudsen does. (See fig. 1 & col. 2, lines 14-25) Knudsen discloses a digital phase lock loop that computes the time difference of the clock input and the clock output.

Therefore, taking the combined teachings of Girardeau, Wong & Knudsen as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system Girardeau, as modified by Wong, in the manner as claimed, and as taught by Knudsen, for the benefit of providing useful information to a filter, which will be later on, to achieve synchronization. (See col. 2, lines 20-25)

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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